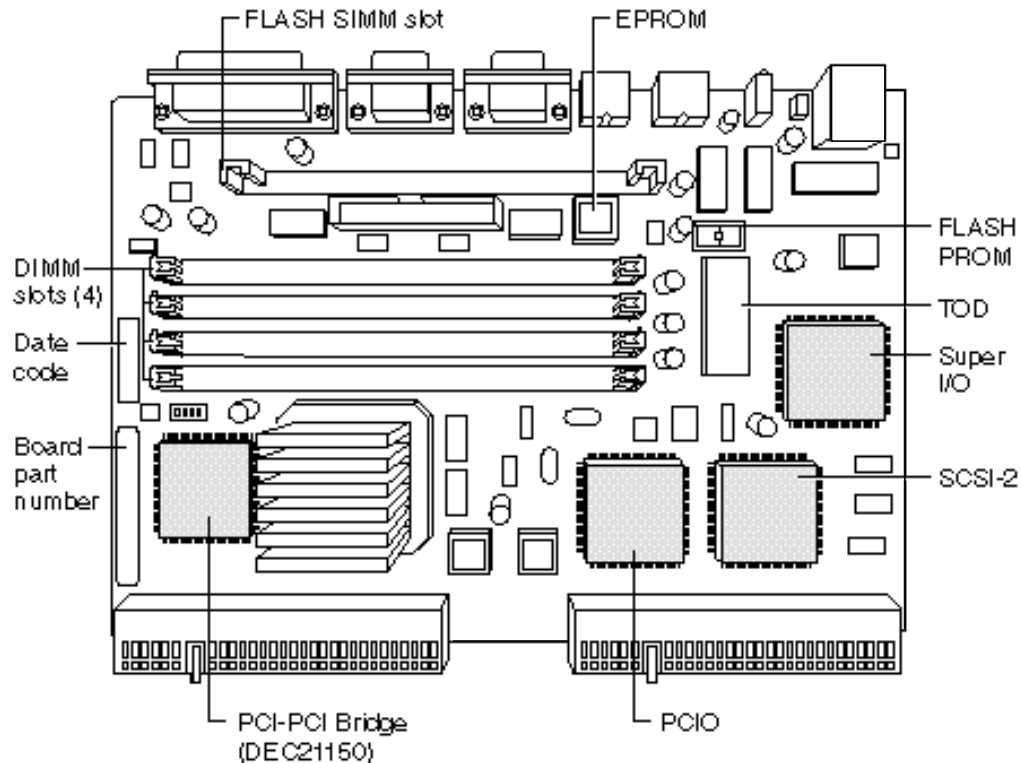


SPARCengine

SPARCengine CP 1200

501-4474
Up to 128MB
100MHz



Note –

1. CP 1200 board requires *no* jumper settings for normal operation.
2. CP 1200 board uses the highly-integrated microSPARC-IIep microprocessor.
3. CP 1200 memory subsystem consists of flash PROM, flash SIMMs, and main memory DIMMs.
4. Two types of flash memory are used:
 - a. One is a 1MB 8-bit wide flash chip that directly interfaces to the microSPARC-IIep processor on the PROM bus.
 - b. The other is a flash memory SIMM socket that can contain 1 MB, 2 MB, and 4 MB SIMMs. The CP 1200 provides the socket; the user must provide the flash SIMM device.
5. Four 168-pin DIMM sockets house up to 128MB of buffered main memory.

SPARCengine CP 1200

501-4474

Up to 128MB

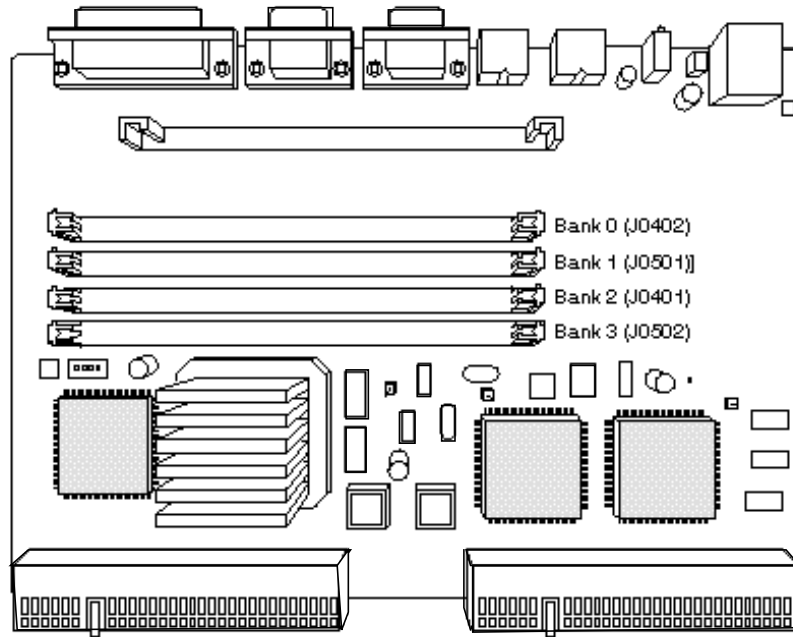
100MHz

Note – Continued

6. 32-bit PCI bus complies with Peripheral Component Interconnect version 2.1 standards developed by Intel® Corporation.
7. Optional 80-pin JEDEC standard flash SIMM socket is for user-defined functions.
8. Up to seven other PCI cards can be installed through the use of the industry standard 32-bit CompactPCI bus.
9. DEC21150 PCI-to-PCI Bridge allows nine additional PCI devices to be used with the host system card. The SPARCengine CP 1200 board is configured to support only seven additional devices.

SPARCengine CP 1200

501-4474 Memory DIMMs



Note –

1. Available DIMM size types are 8MB and 32MB.
2. 16MB DIMMs are also supported, but are not currently manufactured.
3. CP 1200 uses 3.3 V, 168-pin, *buffered* DIMMs only.

Caution – You cannot use unbuffered DIMMs from other Sun board products.

4. CP 1200 memory map requires installing a single DIMM into bank 0 (J0402).

Caution – A DIMM must always be installed in bank 0 for proper operation.

5. Starting address in each slot is the same regardless of the size of DIMM used, but there will not be contiguous areas of memory if DIMMs smaller than 32MB are installed.
6. PROM is pin-selected via jumper inputs to the microSPARC-IIep through two boot mode pins, BM_SEL[1:0], which must be set to one of the values in the table.

BM_SEL[1:0]	Action
0 0	Boot from 32-bit flash PROM (SIMMs) on local memory bus (cacheable after boot).
0 1	Boot from 8-bit flash PROM (local flash chip) on local memory bus (cacheable after boot).

SPARCengine CP 1200

501-4474

Allowable Memory Configurations

Total Memory (MBytes)	Number of DIMMs Used		
	8MB DIMMs	16MB DIMMs	32MB DIMMs
32	4	2	1
40	3 1 1	1 2	1
48	2	3 1	1 1
56	1	1	1
64		4 2	1 2
72	1 1	2	1 2
80		1	2
88	1	1	2
96			3
104	1		3
112		1	3
128			4

Note –

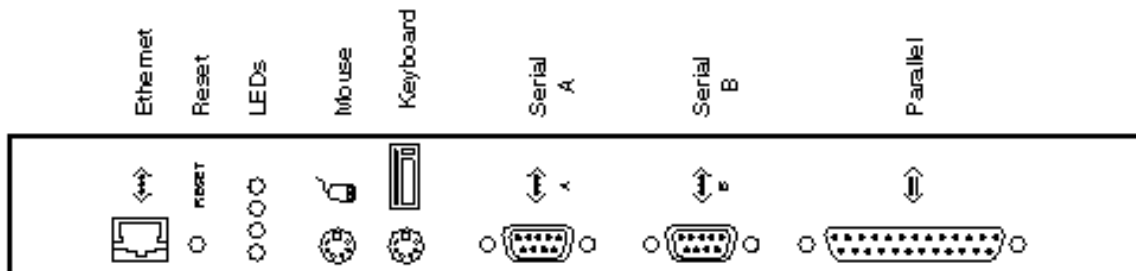
1. All DRAM must be of a speed rating consistent with the target design speed. Recommended access time (for 100 MHz CPU operation) is 60 nanoseconds.
2. All DIMMs must be arranged as 72 bits wide (not 64 bits), and must operate at 3.3 V, have 168 pins, and be buffered.

Caution – Maximum DIMM density per board is 32 MB. Use of any DIMM larger than 32 MB may produce unpredictable results.

SPARCengine CP 1200

501-4474

CP 1200 Board I/O Connections

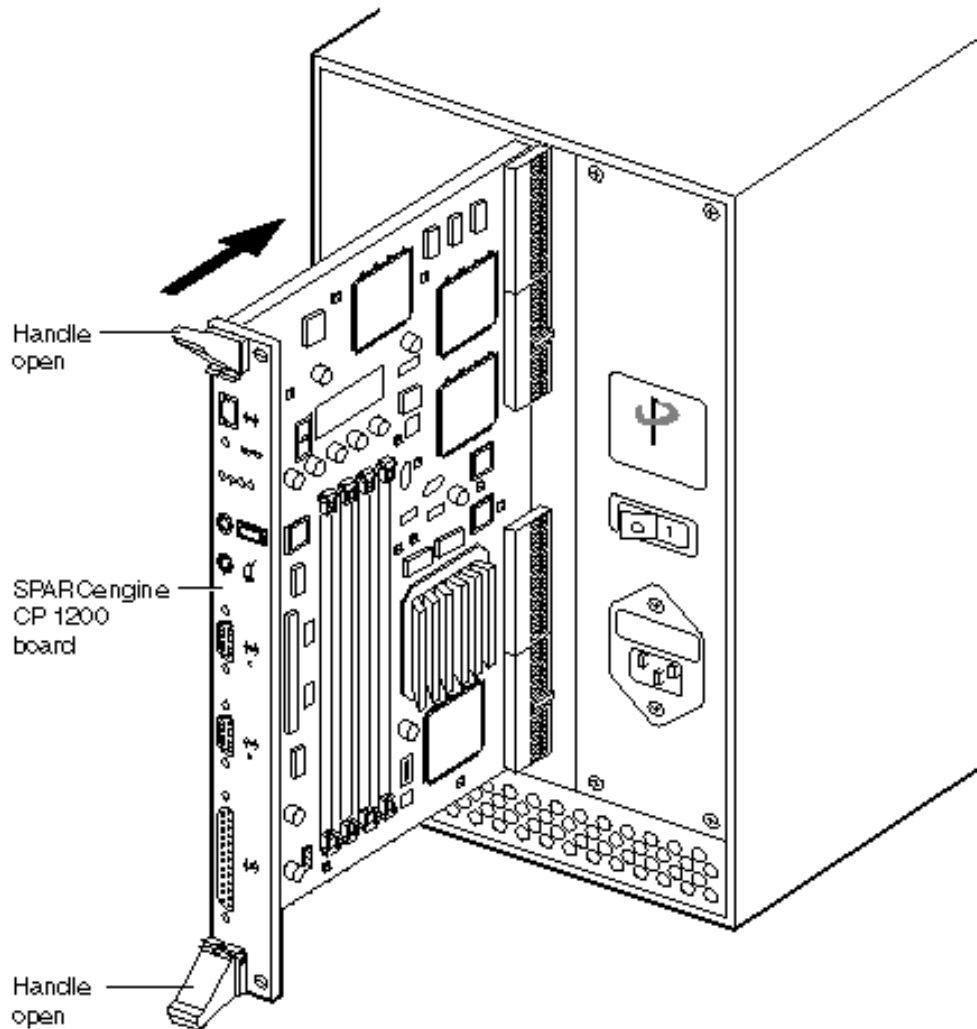


Note –

1. Serial ports are 9-pin plug (male) connectors, providing the standard RS-232 connection.
2. Parallel port is the standard PC-style 25-pin receptacle (female) connector with IEEE 1284 interface.
3. Keyboard and mouse are PS/2-style (6-pin mini-DIN) connectors.
4. Ethernet uses RJ45 connector with 10/100 Mbit autosensing support.
5. Status LEDs (4) indicate:
 - Power - green
 - Ethernet - yellow
 - Two yellow LEDs are user-defined
6. Reset device (Dallas Semiconductor DS1834A) monitors both 3.3 V and 5 V power for proper voltage ranges, and generates CPU_RST_L output that directly resets the microSPARC-IIep CPU and the SuperIO chip.
7. After a board reset (level 1 or power reset), microSPARC-IIep generates a reset to the PCIO and the Ethernet PHY.

SPARCengine CP 1200

501-4474
CP 1200 Board



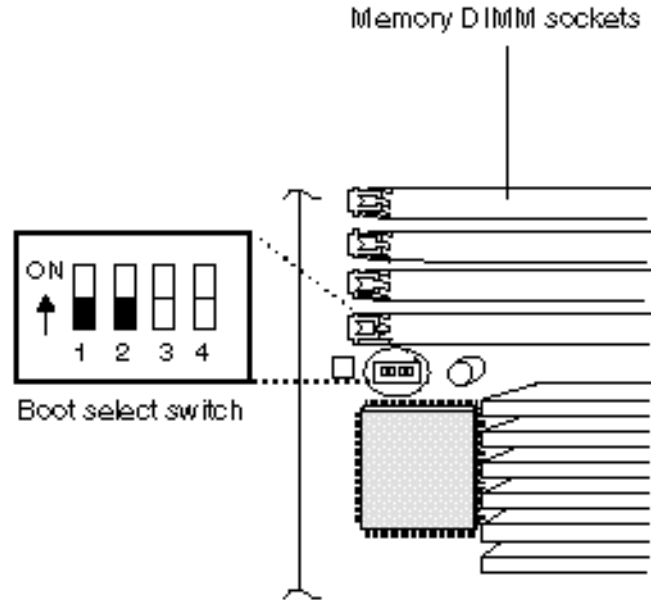
Note –

1. CP 1200 is delivered in a CompactPCI 6U form-factor.
 2. CompactPCI board uses high-quality 2-mm pin and socket connector and can be front-loaded into a rack mount system.
-
1. CP 1200 board requires double-wide 6U slot and 100 watt power supply.
 2. You can only install one CP 1200 board into a single CompactPCI chassis.

Caution – You cannot “hot swap” or install CompactPCI boards while the system is in operation. To change or swap out boards, the SPARCengine CP 1200 must first be shut down.

SPARCengine CP 1200

501-4474 Boot Select Switch



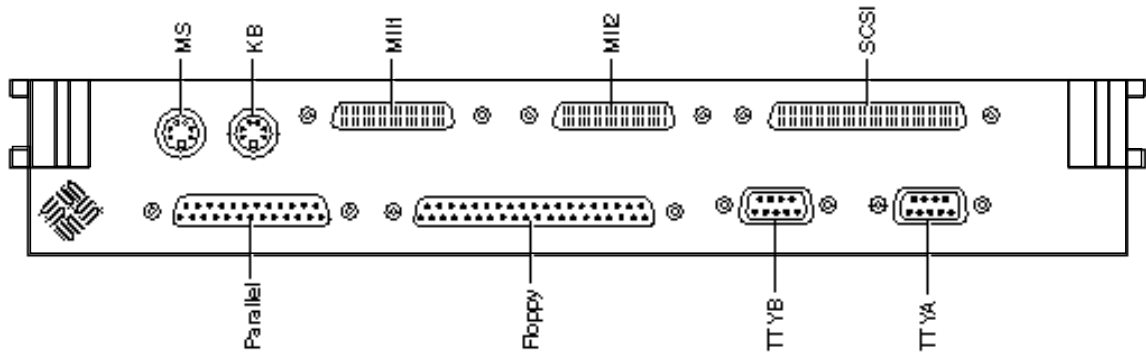
Note –

1. Boot-up switch enables the user to select boot device for CP 1200.
2. CP 1200 boot default setting is from the PROM flash chip.

Boot Device	Switch 1	Switch 2	Switch 3	Switch 4
Flash SIMM	ON	ON	Don't care	Don't care
EPROM	OFF	ON	Don't care	Don't care
SROMBO (not available)	ON	OFF	Don't care	Don't care
PROM flash (default setting)	OFF	OFF	Don't care	Don't care

SPARCengine CP 1200

501-4474
CP1200XBe Transition Module Board



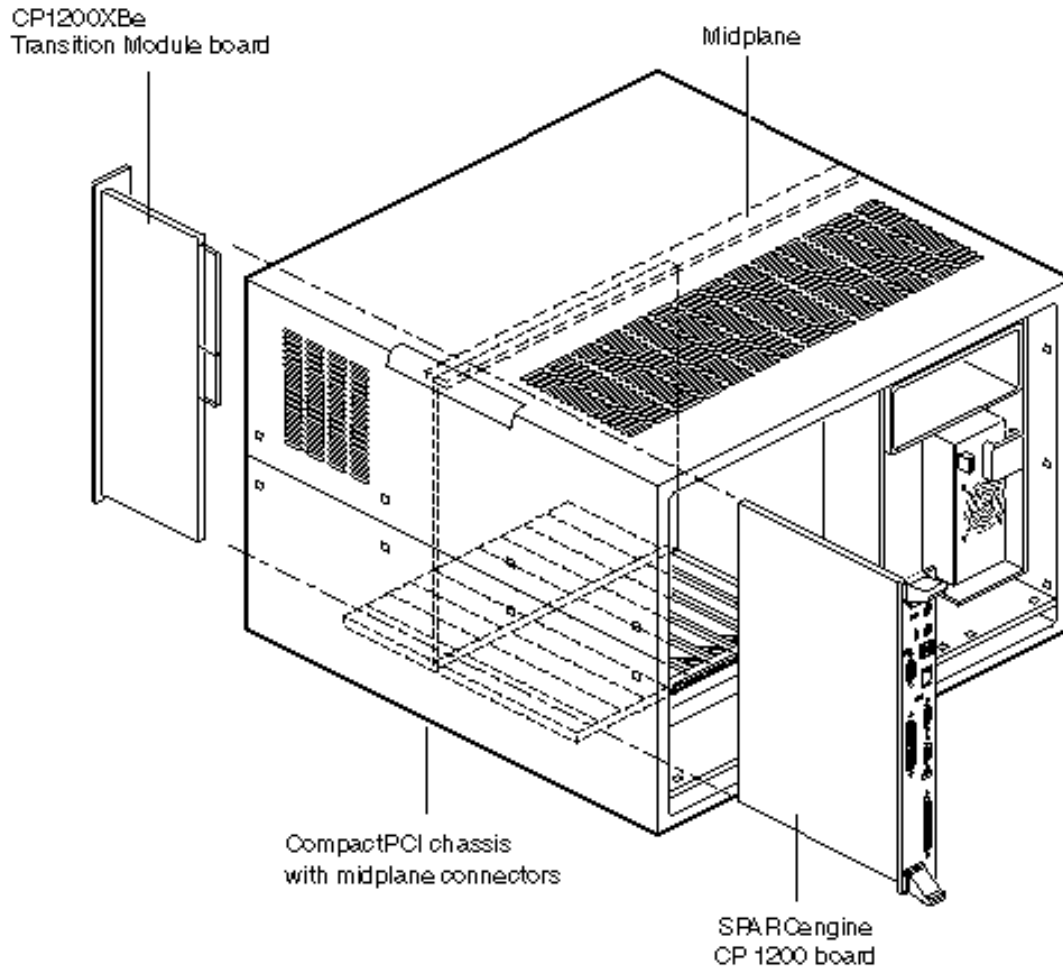
Note –

1. CP1200XBe Transition Module board from Continuous Computing Corporation requires special CompactPCI chassis with a mid-plane that accommodates front and rear CompactPCI board installation.
2. Primary purpose of this board is to provide connection to an external SCSI drive.

SPARCengine CP 1200

501-4474

Compact PCI Chassis

**Note –**

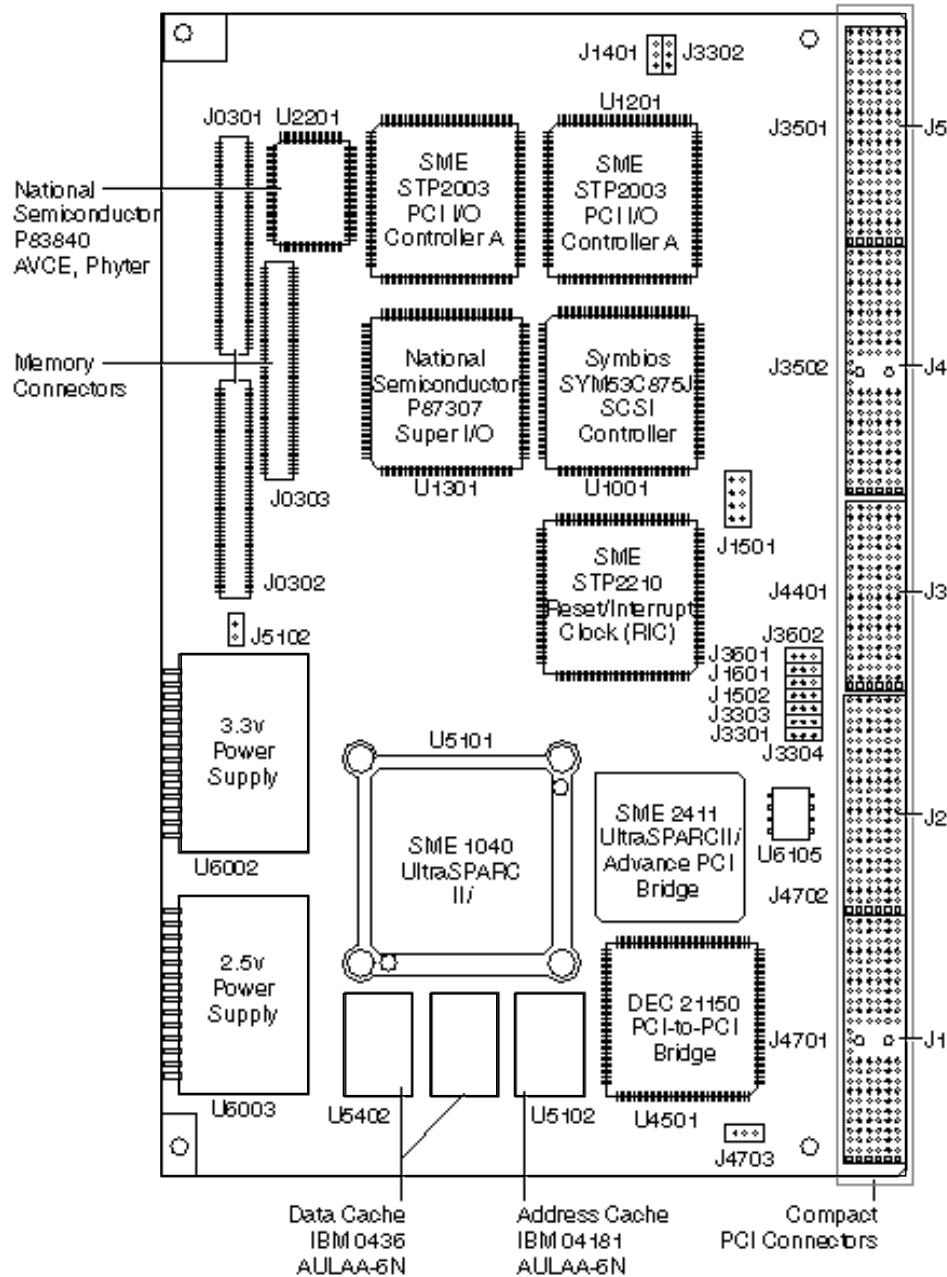
1. Transition Module board must be installed in rear panel slot directly in back of CP 1200 board for proper operation.
2. These back-to-back slots share common pins to enable signal passing from one board to the other.

SPARCengine CP 1500

501-5SS210

64MB 128MB 256MB

270MHz 333MHz



Note –

1. Operates under Solaris 2.6 5/98 or later.
2. Uses UltraSPARC IIi 270 MHz or 333 MHz processor.
3. Supports up to 256MB ECC memory (64MB minimum).

SPARCengine CP 1500

501-5210

64MB 128MB 256MB

270MHz 333MHz

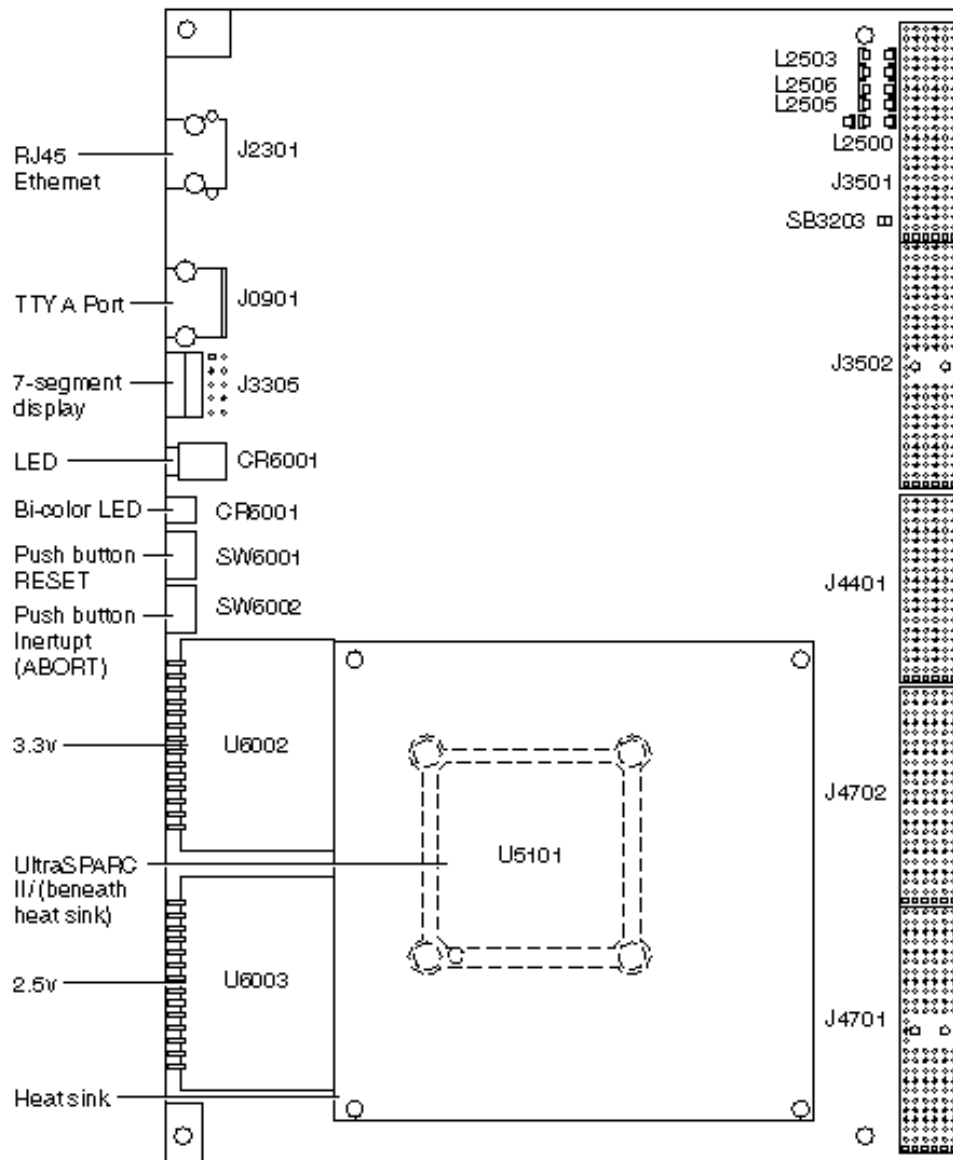
Note – Continued

4. Memory is stackable DRAM modules, up to two modules in single slot configuration.
5. CP 1500 board provides signals for SCSI, Ethernets, ROM emulation, serial ports, parallel port, floppy port, and one PS2 keyboard/mouse.
6. Evaluation Transition Board from Continuous Computer Corporation provides the interfaces for the devices in number 5 above. This board must be ordered separately.
7. Keyboard and mouse connections are supported through the Compact PCI interface J5 connector.

SPARCengine CP 1500

501-5210

Front Panel Components



Note –

1. Front panel interface on serial port A is provided for monitor output. No provision has been made to safeguard the CP 1500 against data entry from the front panel interface.

Caution – If data is simultaneously input through the front panel serial port (Evaluation Transition Board) and the rear panel accesses to serial port A, unpredictable events will occur on the CP 1500 board.

SPARCengine CP 1500

501-5210

Front Panel Components

Note – Continued

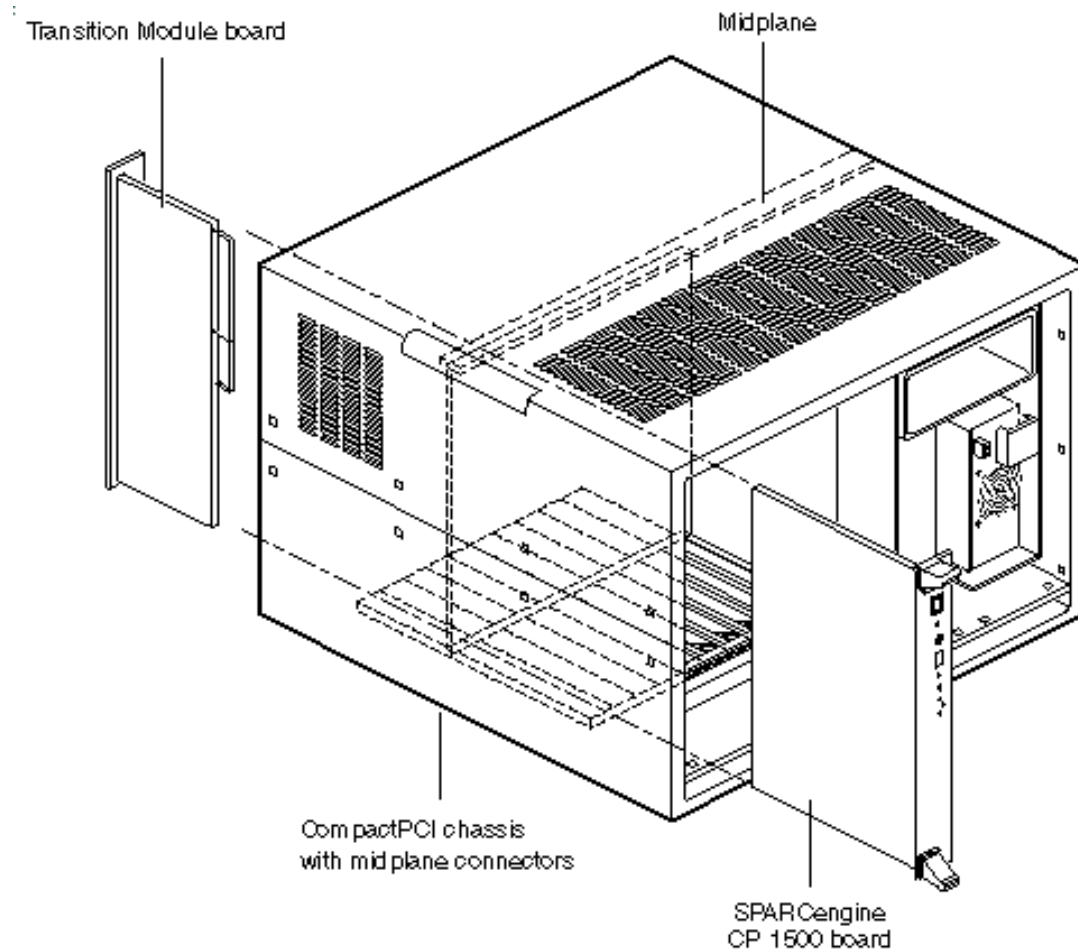
2. CP 1500 supports two 10/100 Mbps Ethernets named A and B. Ethernet A is driven to both the back plane via the MII (on the J4 connector) and front panel via the TPE-RJ45 interface. Ethernet B is driven only to the back plane via MII.
3. ABORT switch is used to break out of a lock-up condition during booting. It is the equivalent of an XIR reset.
4. RESET switch is used to perform a POR (Power On Reset) reset.

Caution – Do not simultaneously assert the RESET and the ABORT

SPARCengine CP 1500

501-5210

Installation of Evaluation Transition Board

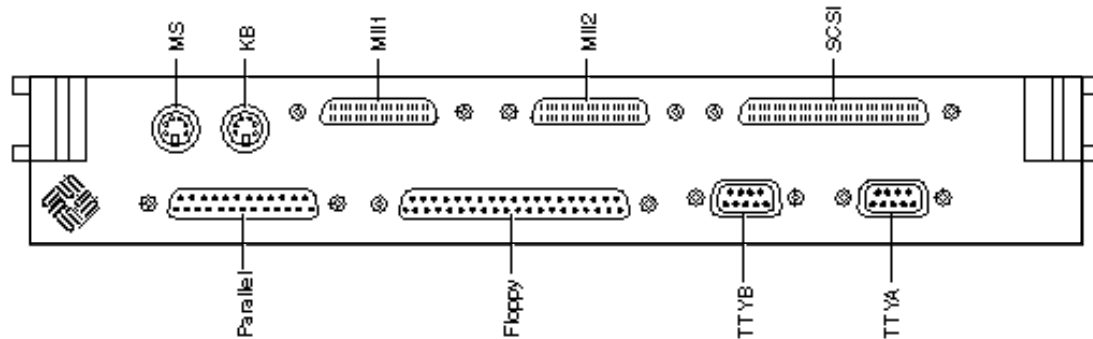
**Note –**

1. CP 1500 board requires a single-wide 6U slot and power supply.
2. All CPCI backplanes/enclosures have one system slot identified by a triangle and up to seven peripheral slots identified by a circle.
3. Evaluation Transition Board must be installed in the rear panel slot directly in back of the CP 1500 board.
4. These back-to-back slots share common pins to enable signal passing from one board to the other.

SPARCengine CP 1500

501-5210

Evaluation Transition Board Ports



Note –

1. Evaluation Transition Board provides connection to all CP 1500 I/O devices.
2. CP 1500 SCSI implementation provides a fast, wide, single-ended, 16-bit data bus with a maximum transfer rate of 40 MB per second.
3. Evaluation Transition Board Jumper Settings:

Jumper	Setting		Default
J0603 and J0605	Open (Not Installed)	TTY A is RS422	
	Short (Installed)	TTY A is RS232	✓
J0604 and J0606	Open (Not Installed)	TTY B is RS422	
	Short (Installed)	TTY B is RS232	✓
J0902	Open (Not Installed)	Ethernet Port A Disabled	
	Short (Installed)	Ethernet Port A Enabled	✓

SPARCengine CP 1500

501-5210

CP 1500 Jumper Settings

Jumper	Setting		Default
J1401	2-3	Enable Flash Write	✓
	1-2	Disable Flash Write	
J1501	1-2	Tclock	No Setting
	2-3	Scan Tclock	
J1502	2-3	Scan Clock	No Setting
	1-2	External Clock	
J1601	1-2	PCI Clock 66/33	No Setting
	2-3	PCI Clock 33/33	
J3301	2-3	Enable Loopback Reset	No Setting
	1-2	Disable Loopback Reset	
J3302	2-3	Enable User Flash Write	No Setting
	1-2	Disable User Flash Write	
J3303	2-3	Boot from ROM Emulator	✓
	1-2	Boot from System Flash	
J3304	3-2	Enable Boot from User Flash	No Setting
	1-2	Disable Boot from User Flash	
J3601	2-3	Enable RAS Feature	✓
	Open	Disable RAS Feature	
J3602	2-3	Enable RAS Feature	✓
	Open	Disable RAS Feature	
J4703	1-2	PLD TDO	No Setting
	2-3	CPCI TDO	
J5102	None	Thermal Diode	No Setting

