

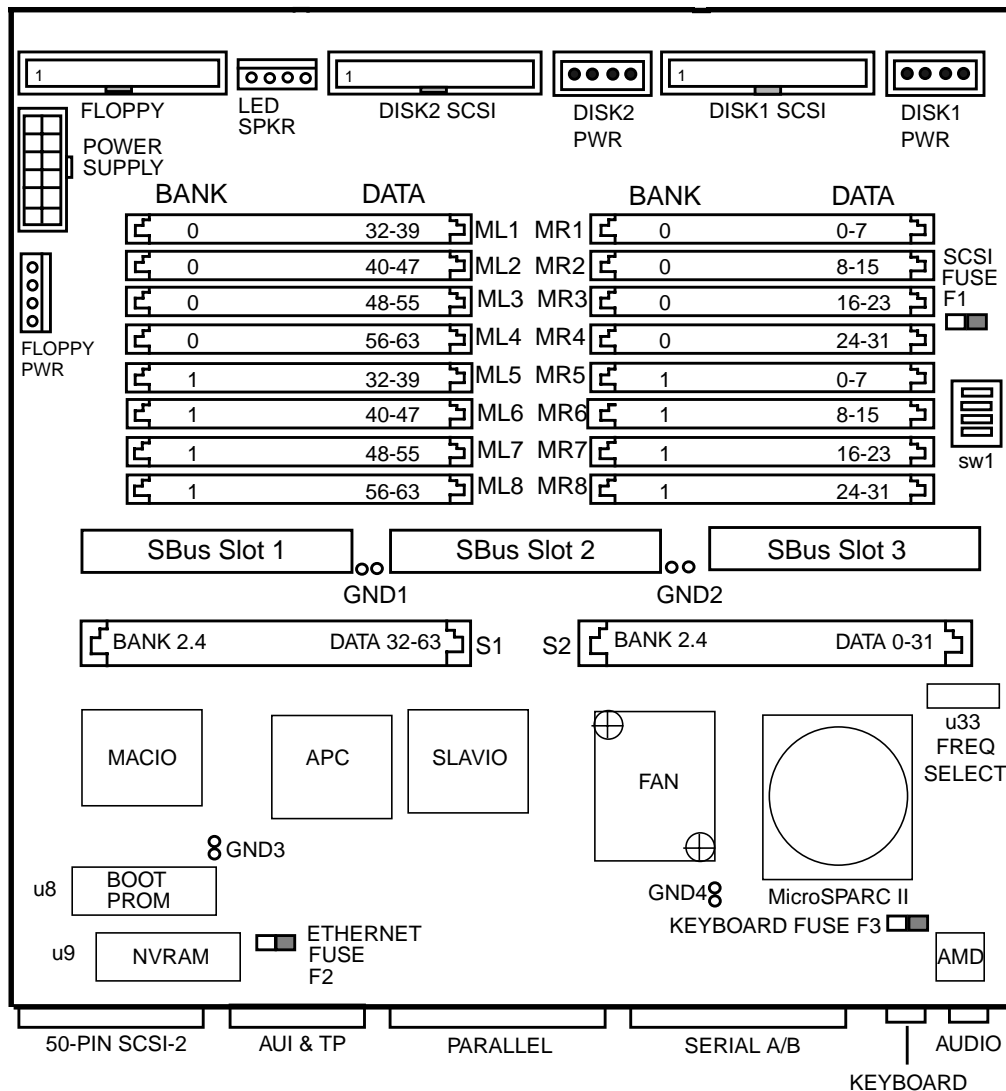
# Cycle5

# Cycle5-SS

370-2335

0MB FRU

70MHz, 85MHz, 90MHz, 100MHz, 110MHz



## Note –

1. AMD supplies 8 bit audio to backplane.
2. Serial A/B uses SS10 style Y cable.
3. Use 72 pin IPX, IPC, Classic style memory in S1 and S2.
4. Use 30 pin SPARCstation1, 1+ & 2 style memory in ML 1-8 MR1-8.
5. FREQ SELECT GAL at U33 selects 70MHz to 110MHz frequency
6. Solaris 2.3/SunOS 5.3 or Solaris 1.1.1 Version B/SunOS 4.1.4 is required.

# Cycle5-SS

## 370-2335

### Supported Memory

Sun supported memory for the different frequency Cycle boards.

SIZE	SIMM SUN P/N	SPEED	CYCLE 5 70-90 MHz	CYCLE 5 100-110 MHz	CYCLE 5 125 MHz
30 PIN					
1MB	501-1408	100ns	X		
1MB	501-1697	80ns	X		
4MB	501-1625	100ns	X		
4MB	501-1739	80ns	X	X	
72 PIN					
4MB	501-1812	80ns	X	X	
4MB	501-1991	60ns	X	X	X
16MB	501-1822	80ns	X	X	
16MB	501-1915	80ns	X	X	
16MB	501-2059	60ns	X	X	X

Physical Layout of memory as reported by POST .

BANK #	REPORTED CAPACITY	MEMORY LOCATION	INDIVIDUAL SIMM CAPACITY	P/N	MAX MEM	PHYSICAL SLOT LOCATION
BANK 0	8MB	8 SETS OF 1MB, 30 PIN SIMMS ML1 TO ML4 & MR1 TO MR4	1MB	501-1697 501-1408	8MB	8 PHYSICAL 30 PIN SLOTS LABELED ML1 TO ML4 AND MR1 TO MR4
BANK 0	32MB	8 SETS OF 4MB, 30 PIN SIMMS ML1 TO ML4 & MR1 TO MR4	4MB	501-1625 501-1739	32MB	
BANK 1	8MB	8 SETS OF 1MB, 30 PIN SIMMS ML5 TO ML8 & MR5 TO MR8	1MB	501-1697 501-1408	8MB	8 PHYSICAL 30 PIN SLOTS LABELED ML5 TO ML8 AND MR5 TO MR8
BANK 1	32MB	8 SETS OF 4MB, 30 PIN SIMMS ML5 TO ML8 & MR5 TO MR8	4MB	501-1625 501-1739	32MB	
BANK 2	8MB	2 SETS OF 4MB, 72 PIN SIMMS S0 TO S1	4MB	501-1812 501-1991	8MB	2 PHYSICAL 72 PIN SLOTS LABELED S0 AND S1
BANK 2	32MB	2 SETS OF 16MB, 72 PIN SIMMS S0 TO S1	16MB	501-1915 501-1822 501-2059	32MB	

**Note** – To obtain reported memory capacity the NVRAM parameter **diag-switch?** is set to true, forcing a diagnostic power on.

# Cycle5-SS

## 370-2335

### DIP Settings

The FREQ SELECT GAL located at U33 sets the maximum microSPARC II frequency with up to three additional lower frequencies selectable via DIP SW1, PINS 3 AND 4.

DIP	PINS	SETTING	DESCRIPTION 70MHz FREQ GAL	DESCRIPTION 85MHz FREQ GAL	DESCRIPTION 90MHz FREQ GAL
SW1	3	OFF*	70MHz	85MHz	90MHz
	4	OFF*	SBus23.3MHz	SBus21.25MHz	SBus22.5MHz
	3	ON	70MHz	70MHz	90MHz
	4	OFF	SBus23.3MHz	SBus23.3MHz	SBus22.5MHz
	3	OFF	70MHz	70MHz	85MHz
	4	ON	SBus23.3MHz	SBus23.3MHz	SBus21.25MHz
	3	ON	70MHz	70MHz	70MHz
	4	ON	SBus23.3MHz	SBus23.3MHz	SBus23.3MHz
DIP	PINS	SETTING	DESCRIPTION 100MHz FREQ GAL	DESCRIPTION 110MHz FREQ GAL	
SW1	3	OFF*	100MHz	110MHz	
	4	OFF*	SBus22.5MHz	SBus22MHz	
	3	OFF	90MHz	100MHz	
	4	ON	SBus22.5MHz	SBus22.5MHz	
	3	ON	85MHz	90MHz	
	4	OFF	SBus21.25MHz	SBus22.5MHz	
	3	ON	70MHz	85MHz	
	4	ON	SBus23.3MHz	SBus21.25MHz	

\*Default Setting for the Cycle5-SS

# Cycle5-SS

## 370-2335

### Jumper/DIP Settings-Continued

The DIP SW1, PINS 1 and 2 control the microSPARC II controller wait states, with the following settings.

JUMPER/DIP	PINS	SETTING	DESCRIPTION
SW1	1	OFF*	spd_sel<0>=0 spd_sel<1>=0
	2	OFF*	
	1	ON	spd_sel<0>=0 spd_sel<1>=1
	2	OFF	
	1	OFF	spd_sel<0>=1 spd_sel<1>=0
	2	ON	
	1	ON	spd_sel<0>=1 spd_sel<1>=1
	2	ON	
GND1	N/A	N/A	GROUND TEST POINT
GND2	N/A	N/A	GROUND TEST POINT
GND3	N/A	N/A	GROUND TEST POINT
GND4	N/A	N/A	GROUND TEST POINT

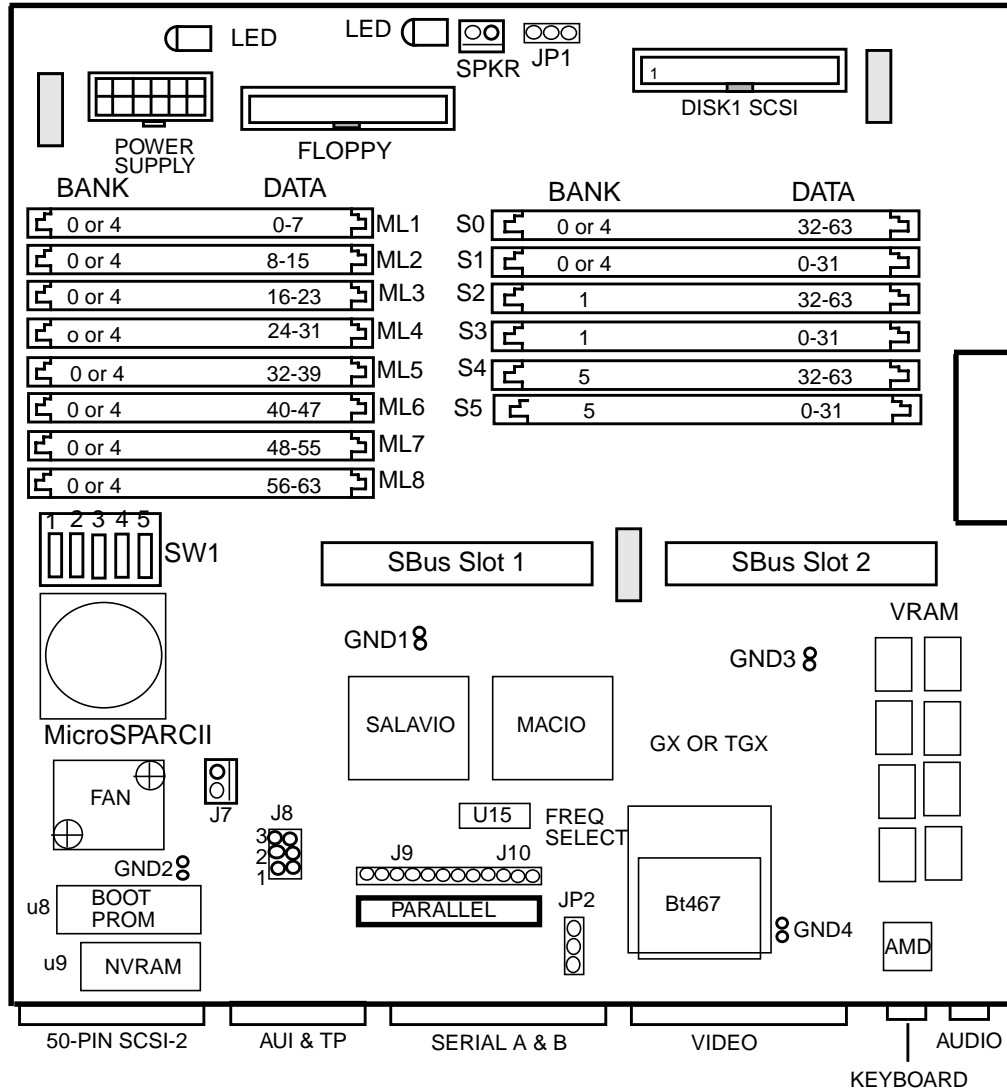
\* Default setting for the Cycle5-SS

# Cycle5-IP

370-2336

0MB FRU

70MHz, 85MHz, 90MHz, 100 MHz, 110MHz



## Note –

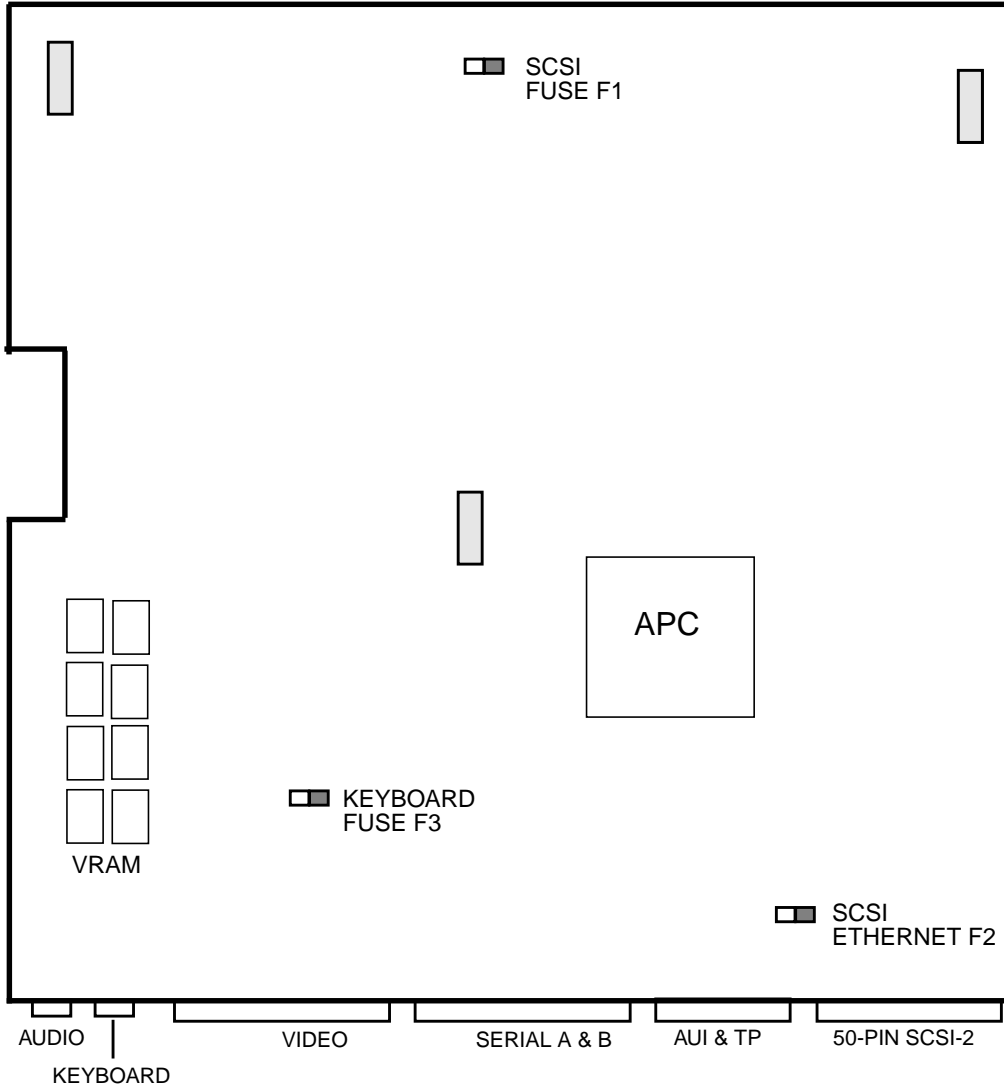
1. AMD supplies 8 bit audio to backplane.
2. Use 72 pin IPX, IPC, Classic style memory in S0 TO S5
3. Use 30 pin SPARCstation1, 1+ & 2 style memory in M1 TO M8
4. FREQ SELECT GAL at U15 selects 70MHz to 110MHz frequency.
5. J8, RS232 1&2 jumpered; RS423 2&3 jumpered
6. Supports BOOTPROM Cycle 5. OBP-B, C, D or E
7. Solaris 2.3/SunOS 5.3 or Solaris 1.1.1 Version B/SunOS 4.1.4 is required.

# Cycle5-IP

370-2336

0MB FRU

70MHz, 85MHz, 90MHz, 100 MHz, 110MHz



REAR VIEW OF BOARD SHOWING FUSES AND APC

# Cycle5-IP

370-2336 370-2334

Physical Layout of memory as reported by POST

DIP SW1 #5 ON (Usually for IPX Upgrades)

(Bank 0 boots from two 72 pin SIMM's in location SO TO S1)

BANK#	REPORTED CAPACITY	MEMORY LOCATION	INDIVIDUAL SIMM CAPACITY	P/N	MAX MEM	PHYSICAL SLOT LOCATION
BANK 4	8MB	8 SETS OF 1MB, 30 PIN SIMMS M1 TO M8	1MB	501-1697 501-1408	8MB	8 PHYSICAL 30 PIN SLOTS LABELED M1 TO M8
BANK 4	32MB	8 SETS OF 4MB, 30 PIN SIMMS M1 TO M8	4MB	501-1625 501-1739	32MB	
BANK 0	8MB	2 SETS OF 4MB, 72 PIN SIMMS S0 TO S1	4MB	501-1812 501-1991	8MB	2 PHYSICAL 72 PIN SLOTS LABELED S0 TO S1
BANK 0	32MB	2 SETS OF 16MB, 72 PIN SIMMS S0 TO S1	16MB	501-1915 501-1882 501-2059	32MB	
BANK 1	8MB	2 SETS OF 4MB, 72 PIN SIMMS S2 TO S3	4MB	501-1812 501-1991	8MB	2 PHYSICAL 72 PIN SLOTS LABELED S2 TO S3
BANK 1	32MB	2 SETS OF 16MB, 72 PIN SIMMS S2 TO S3	16MB	501-1915 501-1822 501-2059	32MB	
BANK 5	8MB	2 SETS OF 4MB, 72 PIN SIMMS S4 TO S5	4MB	501-1812 501-1991	8MB	2 PHYSICAL 72 PIN SLOTS LABELED S4 TO S5
BANK 5	32MB	2 SETS OF 16MB, 72 PIN SIMMS S4 TO S5	16MB	501-1915 501-1822 501-2059	32MB	

DIP SW1 #5 OFF (Usually for IPC Upgrades)

(Bank 0 boots from eight 30 pin SIMM's in location M1 TO M8)

BANK#	REPORTED CAPACITY	MEMORY LOCATION	INDIVIDUAL SIMM CAPACITY	P/N	MAX MEM	PHYSICAL SLOT LOCATION
BANK 0	8MB	8 SETS OF 1MB, 30 PIN SIMMS M1 TO M8	1MB	501-1697 501-1408	8MB	8 PHYSICAL 30 PIN SLOTS LABELED M1 TO M8
BANK 0	32MB	8 SETS OF 4MB, 30 PIN SIMMS M1 TO M8	4MB	501-1625 501-1739	32MB	
BANK 4	8MB	2 SETS OF 4MB, 72 PIN SIMMS S0 TO S1	4MB	501-1812 501-1991	8MB	2 PHYSICAL 72 PIN SLOTS LABELED S0 TO S1
BANK 4	32MB	2 SETS OF 16MB, 72 PIN SIMMS S0 TO S1	16MB	501-1915 501-1882 501-2059	32MB	
BANK 1	8MB	2 SETS OF 4MB, 72 PIN SIMMS S2 TO S3	4MB	501-1812 501-1991	8MB	2 PHYSICAL 72 PIN SLOTS LABELED S2 TO S3
BANK 1	32MB	2 SETS OF 16MB, 72 PIN SIMMS S2 TO S3	16MB	501-1915 501-1822 501-2059	32MB	
BANK 5	8MB	2 SETS OF 4MB, 72 PIN SIMMS S4 TO S5	4MB	501-1812 501-1991	8MB	2 PHYSICAL 72 PIN SLOTS LABELED S4 TO S5
BANK 5	32MB	2 SETS OF 16MB, 72 PIN SIMMS S4 TO S5	16MB	501-1915 501-1822 501-2059	32MB	

# Cycle5-IP

## 370-2336 370-2334 DIP Settings

The FREQ SELECT GAL located at U15 sets the maximum microSPARC II frequency with up to three additional lower frequencies selectable via DIP SW1, PINS 3 AND 4.

DIP	PINS	SETTING	DESCRIPTION 70MHz FREQ GAL	DESCRIPTION 85MHz FREQ GAL	DESCRIPTION 90MHz FREQ GAL
SW1	3	OFF*	70MHz	85MHz	90MHz
	4	OFF*	SBus23.3MHz	SBus21.25MHz	SBus22.5MHz
	3	ON	70MHz	70MHz	90MHz
	4	OFF	SBus23.3MHz	SBus23.3MHz	SBus22.5MHz
	3	OFF	70MHz	70MHz	85MHz
	4	ON	SBus23.3MHz	SBus23.3MHz	SBus21.25MHz
	3	ON	70MHz	70MHz	70MHz
	4	ON	SBus23.3MHz	SBus23.3MHz	SBus23.3MHz
DIP	PINS	SETTING	DESCRIPTION 100MHz FREQ GAL	DESCRIPTION 110MHz FREQ GAL	
SW1	3	OFF*	100MHz	110MHz	
	4	OFF*	SBus22.5MHz	SBus22MHz	
	3	OFF	90MHz	100MHz	
	4	ON	SBus22.5MHz	SBus22.5MHz	
	3	ON	85MHz	90MHz	
	4	OFF	SBus21.25MHz	SBus22.5MHz	
	3	ON	70MHz	85MHz	
	4	ON	SBus23.3MHz	SBus21.25MHz	

\*Default Setting for the Cycle5-IP

# Cycle5-IP

370-2336 370-2334

## Jumper/DIP Settings-Continued

The DIP SW1, PINS 1 and 2 control the microSPARC II controller wait states, DIP SW1 PIN 5 controls the BANK 0 memory select. Other Jumpers are as follows.

JUMPER/DIP	PINS	SETTING	DESCRIPTION
SW1	1	OFF*	spd_sel<0>=0
	2	OFF*	spd_sel<1>=0
	1	ON	spd_sel<0>=0
	2	OFF	spd_sel<1>=1
	1	OFF	spd_sel<0>=1
	2	ON	spd_sel<1>=0
	1	ON	spd_sel<0>=1
	2	ON	spd_sel<1>=1
SW5	5	OFF	BANK 0 SELECTED TO 30 PIN SIMMS, M1 TO M8
SW5	5	ON*	BANK 0 SELECTED TO 72 PIN SIMMS, S0 TO S1
GND1	N/A	N/A	GROUND TEST POINT
GND2	N/A	N/A	GROUND TEST POINT
GND3	N/A	N/A	GROUND TEST POINT
GND4	N/A	N/A	GROUND TEST POINT
J7			FAN POWER
J8	1 & 2	JUMPERED*	RS232
J8	2 & 3	JUMPERED	RS423
J9			MANUFACTURING TEST JUMPER
J10			MANUFACTURING TEST JUMPER
JP1			MANUFACTURING TEST JUMPER
JP2			MANUFACTURING TEST JUMPER

\*Default Setting for the Cycle5-IP

# Cycle5-IP

## 370-2336 370-2334 Supported Memory

Sun supported memory for the different frequency Cycle boards.

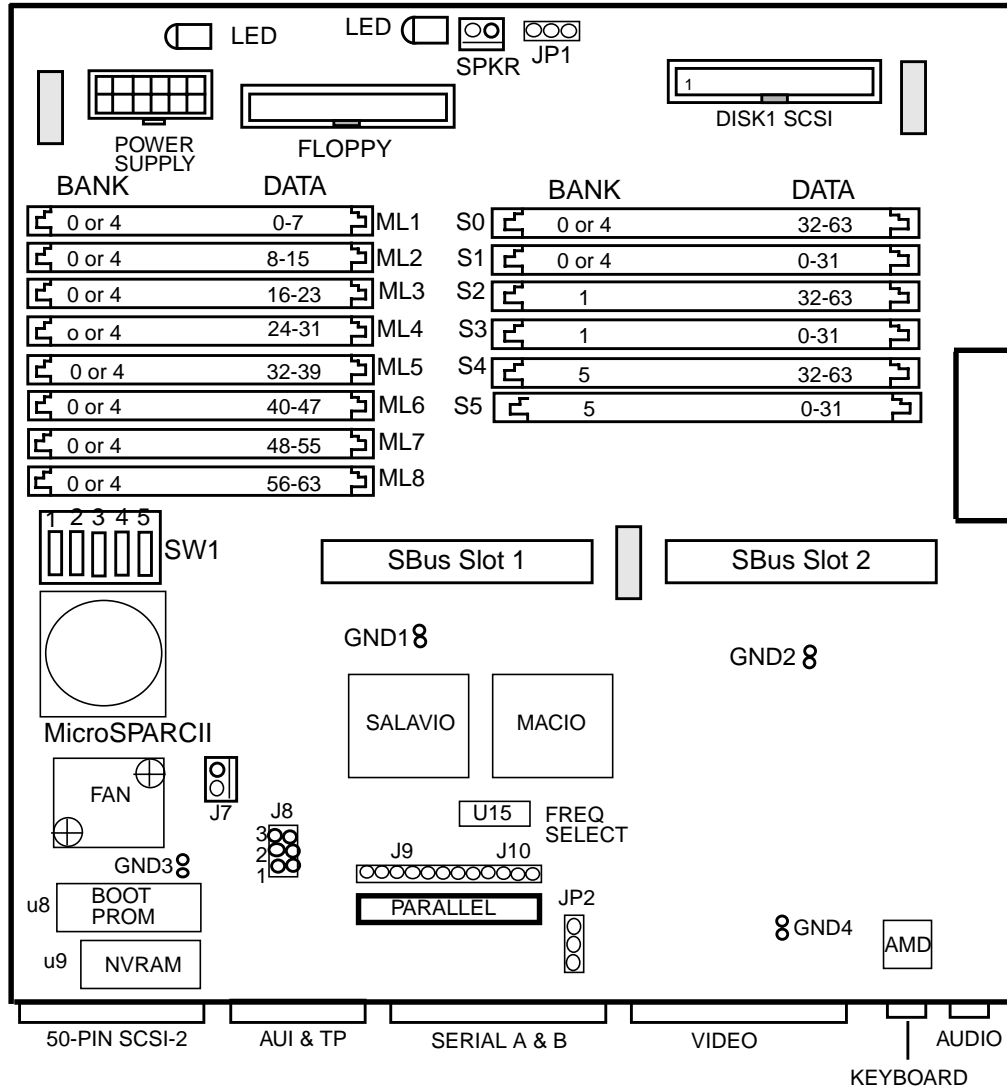
SIZE	SIMM SUN P/N	SPEED	CYCLE 5 70-90 MHz	CYCLE 5 100-110 MHz	CYCLE 5 125 MHz
30 PIN					
1MB	501-1408	100ns	X		
1MB	501-1697	80ns	X		
4MB	501-1625	100ns	X		
4MB	501-1739	80ns	X	X	
72 PIN					
4MB	501-1812	80ns	X	X	
4MB	501-1991	60ns	X	X	X
16MB	501-1822	80ns	X	X	
16MB	501-1915	80ns	X	X	
16MB	501-2059	60ns	X	X	X

# Cycle5-IP-NL-1

370-2334

0MB FRU

70MHz, 85MHz, 90MHz, 100 MHz, 110MHz



## Note –

1. AMD supplies 8 bit audio to backplane.
2. Use 72 pin IPX, IPC, Classic style memory in S0 TO S5
3. Use 30 pin SPARCstation1, 1+ & 2 style memory in M1 TO M8
4. FREQ SELECT GAL at U15 selects 70MHz to 110MHz frequency.
5. J8, RS232 1&2 jumpered; RS423 2&3 jumpered
6. Supports BOOTPROM Cycle 5. OBP-A.
7. Solaris 2.3/SunOS 5.3 or Solaris 1.1.1 Version B/SunOS 4.1.4 is required.